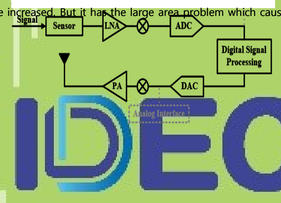
To overcome the

mismatch effect, the size of current source should be increased. But it has the large area problem which causes parasitic and gradient mismatch. Another solution to solve the mismatch effect uses the

Figure 1. Block diagram of sensor network



IDEC Chip Design Contest

An energy efficient current-mode two-tap pre-emphasis output driver using capacitive peaking scheme

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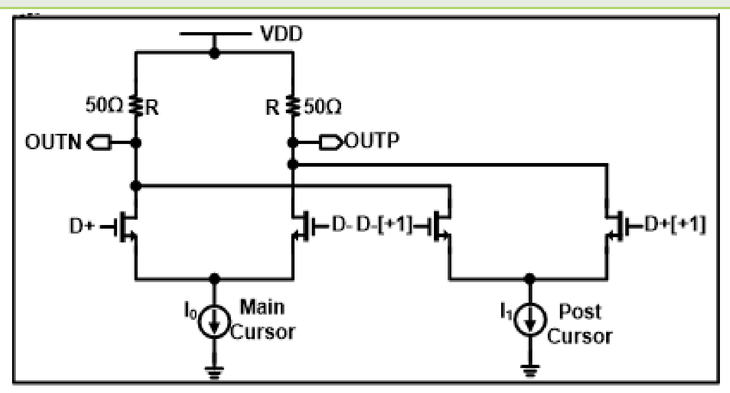
Introduction

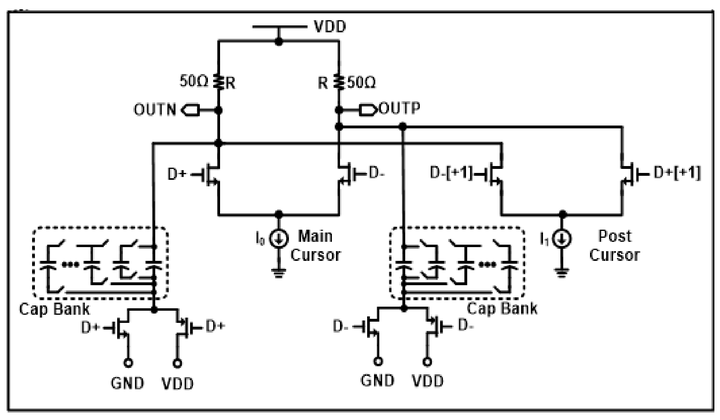
The continual growth in processing power of GPU for machine learning server and the increasing demand for Giga Ethernet services makes a need for higher bandwidth data transmission. In order to satisfy with the need, industrial standards are being developed in terms of the channel characteristics and interface electrical specifications of short channel (on-board) and long channel (inter-card) for serial transmitter at data rates of 10-Gb/s or above, which results in developing package techniques on board for reducing channel loss. However, power efficiency transmitters have to be needed because of the limitation of material for PCB. For high-speed data transmission, there are typically two drivers such as current mode logic (CML) and Source-series-terminated (SST) output driver.

A type of CML output driver is frequently employed because they support high data rates and have an inherently low susceptibility to power supply noise. However, these advantages come along with some drawbacks such as the static power consumption and the inability to support different dc termination. Moreover, the more CML output driver compensates for channel loss, the more the static power consumption increase and the amplitude of output swing decrease. In order to reduce the static power consumption, SST driver, which leads to supporting many different termination voltages combined with a higher signal swing without the static power consumption. As a result, the SST driver is able to reduce power consumption up to 4 times. However, the voltage-mode drivers generally have degraded transmit equalization and Therefore, in this paper, the current-mode output driver having reconfigurable capacitive peaking is proposed for low power consumption and low susceptibility about power supply noise.

Capacitive Peaking Scheme



(a)



(b)

Fig. 1. (a) Schematic of implemented half-rate conventional CML driver and (b) of the proposed one

The proposed output driver is shown in Fig. 1 (b). Capacitor bank that consists of eight capacitors is just added at the node of CML driver output in order to increase the ability to compensate for the channel loss. Unlike the equalization gain of the conventional one, the equalization gain of the proposed pre-emphasis can be varied from 4dB to 15.2dB without increasing the amount of current source for main and post cursor because the proposed uses the energy from the capacitor bank. Based on conservation law, the variation of voltage at the bottom plate capacitor has an effect to the top plate of capacitor, which results in increasing the equalization gain of pre-emphasis. In order to implement this method, the high threshold voltage MOSFET is used. Because the level of swing for CML driver is typically from VDD to the VDD-I X R, it is for MOS switches not to be able to turn on and off. Due to this reason, the switches for capacitive peaking in the proposed pre-emphasis CML driver are realized with high threshold voltage MOSFET. And the pre driver for the switched for capacitive peaking consumes more 1.5 times in order to increase the amplitude of swing. Even if the conventional one dissipates the current and the amplitude of swing in order to increase the ability of equalization gain, the proposed one just adds the pre driver having more power consumption to the output node, which results in reducing the overall power consumption. As shown in Fig. 1 (b), through the pre- driver, the data without 1-UI delay is just connected with the gate of MOS switches. The data in phase is connected with the gate of MOS switches at the OUTN and the data out of phase is connected with that of MOS switches at the OUTP, which causes to charge and discharge at the bottom plate of the capacitor.

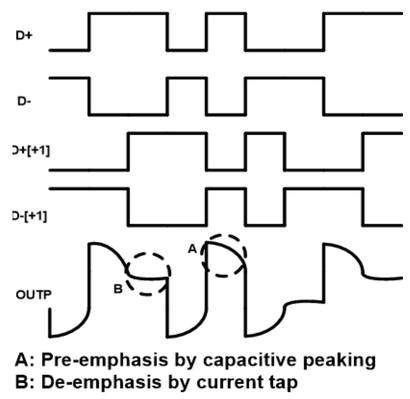
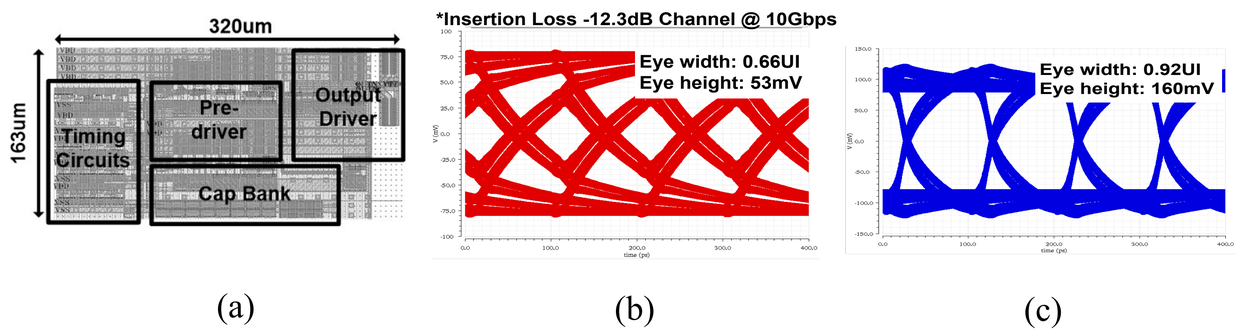


Fig. 2. Operation of proposed CML driver

The operation of the proposed is shown in Fig. 2. When the data in phase is low, the bottom plate of capacitor is charged to VDD. And when the data in phase is high, the bottom plate of capacitor is discharged to GND. This variation at the bottom plate of capacitor increases the gain of pre-emphasis at the OUTN when the output signal is changed from VDD to GND. At the OUTP, the method to increase the gain of pre-emphasis is same. Even if the capacitor bank improves the overall gain of CML driver, the impedance matching may have the problem The unit capacitance is 50fF. In the worst case that the eight capacitances are connected with VDD, the value of effective termination resistance is about 41 ohm. However, the pseudo random binary sequence (PRBS) includes frequency components from low frequency to high frequency domain. The average value of effective termination resistance is almost 50 ohm. Therefore, the total capacitance can be negligible in terms of impedance matching.

Conclusion



(a) (b) (c)

Fig. 3 (a)Layout of the proposed driver, (b) Eye diagram of the conventional one and (c) of the proposed one

Layout of the proposed driver is shown in Fig. 3 (a). As a result, the eye height and width of the proposed driver is clearly improved than the conventional one as shown in Fig 3 (b), (c). An eye height of 160 mV and an eye width of 0.92UI are achieved. The width of eye diagram for the proposed is improved about 28.2% compared with the conventional.

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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